1. A method of using anti-code dosage as LDD implant to turn off a MOS transistor comprising the steps of:

providing a substrate having an NMOS region and a PMOS region;

forming a dielectric layer over said substrate, including over said NMOS and PMOS regions;

forming an NMOS gate electrode over said NMOS region and a PMOS gate electrode over said PMOS region over said dielectric layer formed over said NMOS and PMOS regions;

forming a first cover layer over said PMOS region including over said PMOS gate electrode;

performing an N-type lightly doped drain (NLDD) implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said first cover layer from over said PMOS region;

forming a second cover layer over said NMOS region including over said NMOS gate electrode;

performing P-type lightly doped drain (PLDD) implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said second cover layer from over said NMOS region;

forming a third cover layer over said PMOS region including over said PMOS gate electrode;

performing a code implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said third cover layer from over said PMOS region;

forming a fourth cover layer over said NMOS region including over said NMOS gate electrode;

performing a code implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said fourth cover layer from over said NMOS region; and

performing a vertical anti-code LDD implant to turn off said MOS transistor.

2. The method according to claim 13, wherein said substrate is silicon.

3. The method according to claim 13, wherein said dielectric layer is a gate oxide layer having a thickness between about 100 to 150 angstroms (Å).

4. The method according to claim 13, wherein said NMOS and PMOS gate electrodes comprise a polysilicon layer having a thickness between about 1400 to 1600 Å, a tetraethyl orthosilicate (TEOS) layer having a thickness between about 750 to 850 Å, and a tungsten silicide layer having a thickness between about 1000 to 1500 Å.

5. The method according to claim 13, wherein said NMOS and PMOS gate electrodes comprise polycide which further comprises polysilicon having a thickness between about 1400

to 1600 Å and tungsten silicide having a thickness between about 1200 to 1300 Å.

6. The method according to claim 13, wherein said first cover layer is photoresist having a thickness between about 1.0 to 1.2 micrometers (μm).

7. The method according to claim 1, wherein said performing said NLLD implant over uncovered said NMOS region is accomplished with As ions at a dosage level between about $4x10^{13}$ to $6x10^{13}$ atoms/cm^3 and at an energy level between about 40 to 60 KeV.

8. The method according to claim 1 or 6, wherein said removing said first cover layer is accomplished by oxygen plasma ashing.

9. The method according to claim 1, wherein said performing said PLLD implant over uncovered said PMOS region is accomplished with BF_2 ions at a dosage level between about $1.5x10^{13}$ to $2.0x10^{13}$ atoms/cm^3 and at an energy level between about 20 to 40 KeV.

10. The method according to claim 1, wherein said performing said code implant over uncovered said NMOS

region is accomplished with BF_2 ions at a dosage level between about $9x10^{13}$ to $1x10^{14}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV.

11. The method according to claim 1, wherein said performing said code implant over uncovered said PMOS region is accomplished with P ions at a dosage level between about $6x10^{13}$ to $9x10^{13}$ atoms/cm^3 and at an energy level between about 25 to 35 KeV.

12. The method according to claim 1, wherein said performing said vertical anti-code dosage is accomplished with BF_2 ions at a dosage level between about $4.0x10^{13}$ to $5.0x10^{13}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV.

13. A method of using anti-code dosage as LDD implant to turn off a MOS transistor comprising the steps of:

providing a substrate having an NMOS region and a PMOS region;

forming a dielectric layer over said substrate, including over said NMOS and PMOS regions;

forming an NMOS gate electrode over said NMOS region and a PMOS gate electrode over said PMOS region over said dielectric layer formed over said NMOS and PMOS regions;

forming a first cover layer over said PMOS region including over said PMOS gate electrode;

performing an N-type lightly doped drain (NLDD) implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said first cover layer from over said PMOS region;

forming a second cover layer over said NMOS region including over said NMOS gate electrode;

performing P-type lightly doped drain (PLDD) implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said second cover layer from over said NMOS region;

forming a third cover layer over said PMOS region including over said PMOS gate electrode;

performing a code implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said third cover layer from over said PMOS region;

forming a fourth cover layer over said NMOS region including over said NMOS gate electrode;

performing a code implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said fourth cover layer from over said NMOS region; and

performing a tilt angle anti-code LDD implant to turn off said MOS transistor.

14. The method according to claim 13, wherein said substrate is silicon.

15. The method according to claim 13, wherein said dielectric layer is a gate oxide layer having a thickness between about 10 to 150 angstroms (Å).

16. The method according to claim 13, wherein said NMOS and PMOS gate electrodes comprise a polysilicon layer having a thickness between about 1400 to 1600 Å, a tetraethyl orthosilicate (TEOS) layer having a thickness between about 750 to 850 Å, and a tungsten silicide layer having a thickness between about 1000 to 1500 Å.

17. The method according to claim 13, wherein said NMOS and PMOS gate electrodes comprise polycide which further comprises polysilicon having a thickness between about 1400 to 1600 Å and tungsten silicide having a thickness between about 1200 to 1300 Å.

18. The method according to claim 13, wherein said first cover layer is photoresist having a thickness between about 1.0 to 1.2 micrometers (μm).

19. The method according to claim 13, wherein said performing said NLLD implant over uncovered said NMOS region is accomplished with As ions at a dosage level

between about $4x10^{13}$ to $6x10^{13}$ atoms/cm^3 and at an energy level between about 40 to 60 KeV.

20. The method according to claim 13 or 18, wherein said removing said first cover layer is accomplished by oxygen plasma ashing.

21. The method according to claim 13, wherein said performing said PLLD implant over uncovered said PMOS region is accomplished with BF_2 ions at a dosage level between about $1.5x10^{13}$ to $2.0x10^{13}$ atoms/cm^3 and at an energy level between about 20 to 40 KeV.

22. The method according to claim 13, wherein said performing said code implant over uncovered said NMOS region is accomplished with BF_2 ions at a dosage level between about $9x10^{13}$ to $1x10^{14}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV.

23. The method according to claim 13, wherein said performing said code implant over uncovered said PMOS region is accomplished with P ions at a dosage level between about $6x10^{13}$ to $9x10^{13}$ atoms/cm^3 and at an energy level between about 25 to 35 KeV.

24. The method according to claim 13, wherein said performing said tilt angle anti-code LDD implant is accomplished with BF_2 ions at a dosage level between about $4.0x10^{13}$ to $5.0x10^{13}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV, and at a tilt angle between about 40 to 45 degrees.

25. A method of using anti-code dosage as LDD implant to turn off a MOS transistor comprising the steps of:

providing a substrate having an NMOS region and a PMOS region;

forming a dielectric layer over said substrate, including over said NMOS and PMOS regions;

forming an NMOS gate electrode over said NMOS region and a PMOS gate electrode over said PMOS region over said dielectric layer formed over said NMOS and PMOS regions;

forming a first cover layer over said PMOS region including over said PMOS gate electrode;

performing an N-type lightly doped drain (NLDD) implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said first cover layer from over said PMOS region;

forming a second cover layer over said NMOS region including over said NMOS gate electrode;

performing P-type lightly doped drain (PLDD) implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said second cover layer from over said NMOS region;

forming a third cover layer over said PMOS region including over said PMOS gate electrode;

performing a code implant over uncovered said NMOS region using said NMOS gate electrode as a self-aligned mask;

removing said third cover layer from over said PMOS region;

forming a fourth cover layer over said NMOS region including over said NMOS gate electrode;

performing a code implant over uncovered said PMOS region using said PMOS gate electrode as a self-aligned mask;

removing said fourth cover layer from over said NMOS region; and

performing a vertical and tilt angle anti-code LDD implant to turn off said MOS transistor.

26. The method according to claim 25, wherein said substrate is silicon.

27. The method according to claim 25, wherein said dielectric layer is a gate oxide layer having a thickness between about 100 to 150 angstroms (Å).

28. The method according to claim 25, wherein said NMOS and PMOS gate electrodes comprise a polysilicon layer having a thickness between about 1400 to 1600 Å, a tetraethyl orthosilicate (TEOS) layer having a thickness

between about 750 to 850 Å, and a tungsten silicide layer having a thickness between about 1000 to 1500 Å.

29. The method according to claim 25, wherein said NMOS and PMOS gate electrodes comprise polycide which further comprises polysilicon having a thickness between about 1400 to 1600 Å and tungsten silicide having a thickness between about 1200 to 1300 Å.

30. The method according to claim 25, wherein said first cover layer is photoresist having a thickness between about 1.0 to 1.2 micrometers (μm).

31. The method according to claim 25, wherein said performing said NLLD implant over uncovered said NMOS region is accomplished with As ions at a dosage level between about $4x10^{13}$ to $6x10^{13}$ atoms/cm^3 and at an energy level between about 40 to 60 KeV.

32. The method according to claim 25 or 30, wherein said removing said first cover layer is accomplished by oxygen plasma ashing.

33. The method according to claim 25, wherein said performing said PLLD implant over uncovered said PMOS region is accomplished with BF_2 ions at a dosage level between about $1.5x10^{13}$ to $2.0x10^{13}$ atoms/cm^3 and at an energy level between about 20 to 40 KeV.

34. The method according to claim 25, wherein said performing said code implant over uncovered said NMOS region is accomplished with BF_2 ions at a dosage level between about $9x10^{13}$ to $1x10^{14}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV.

35. The method according to claim 25, wherein said performing said code implant over uncovered said PMOS region is accomplished with phosphorous (P) ions at a dosage level between about $6x10^{13}$ to $9x10^{13}$ atoms/cm^3 and at an energy level between about 25 to 35 KeV.

36. The method according to claim 25, wherein said performing said vertical and tilt angle anti-code LDD implant is accomplished with BF_2 ions at a dosage level between about $4.0x10^{13}$ to $5.0x10^{13}$ atoms/cm^3 and at an energy level between about 35 to 45 KeV, and at a tilt angle between about 40 to 45 degrees.